REMARKS/ARGUMENTS

Claims 1-11 are currently pending in this application. Claims 1, 2, 5, 6, 8, and 9 have been amended to further define the invention. Claims 10 and 11 have been added. No new matter has been included as a result of these amendments. Support for the amendments to the claims may be found in Figures 2 and 3 and the corresponding text.

Rejections under 35 U.S.C. § 103

Claims 1-9 were rejected as being unpatentable over the combination of US Patent No. 6,460,120 to Bass et al. in view of US Patent No. 5,666,494 to Mote Jr. further in view of the IEEE article Gupta et al. In light of the amendments and the arguments contained herein, Applicants respectfully request withdrawal of this rejection.

As acknowledged by the Examiner, Bass fails to disclose or teach the features of the longest prefix match lookup table incorporated into independent claims 1, 5, and 8. The amended features of claims 1, 5, and 8 include a first set of data pairs including a key value and a mask value, the mask value indicating a number of least significant bits that may be ignored within the key value, the first set of pairs being ordered according to corresponding mask values. The Examiner asserts that Gupta discloses multiple lookup tables to increase throughput and Mote discloses using a single row with a large number of columns to increase memory speed. Applicants respectfully submit that Gupta and Mote are silent as to the format of the data pairs or the ordering of the data pairs as specified in claims 1, 5, and 8, as amended. The format entry for Gupta is discussed in Figure 3 and in section 3. One table is used for storing prefixes smaller than 24 bits, while the second table is used for storing prefixes larger than 24 bits. A most significant bit of the value in the table is used to indicate

whether the prefix is smaller or larger than 24 bits (see section 3, Figures 3 and 4 and corresponding text). The table entries of Gupta and the claims, as amended, are wholly unrelated. The Examiner additionally characterizes Mote as disclosing having a large number of columns in a single row to increase memory access speed. Mote discusses the rows of a memory array having a number of columns. Here, Mote is referring to the word lines and bit lines of the memory array. The intersection of these lines define a cell where data may be stored. Mote refers to the fact that in page mode operation, it is easier to access cells along the same row (word line) so that another word line does not have to be activated. The Applicants respectfully request that the Examiner elaborate how the DRAM configuration of Mote is related to a lookup table having data pairs in a single row.

Additionally, Applicants disagree with the Examiner's assertion that one skilled in the art would combine the references as suggested by the Examiner. Gupta refers to a route lookup mechanism implemented in hardware (see abstract). Mote refers to a DRAM control circuit that can post write commands and continue processing without waiting for the write command to complete. According to the Examiner, it would have been obvious to combine Gupta and Mote in order to reduce the access time when searching for a network forwarding address. Gupta discloses a route lookup mechanism that achieves one route lookup every memory access (see abstract). Furthermore, Gupta does not write to the lookup table when performing the route lookup, so one skilled in the art would not look to Gupta as suggested by the Examiner. Applicants respectfully submit that Mote provides no teaching to one skilled in the art to achieve more than one route lookup every access, especially when considering no writes to the lookup table are being performed by Gupta.

With respect to claim 9, Applicants respectfully disagree with the Examiner's characterization of Bass. According to the Examiner, Bass discloses at column 25 line 45 –

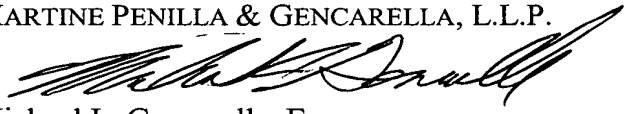
column 26 line5, the features of if one or more entries comprise a same key, a key having a smallest mask is selected, and if no key matches, a maximum key in a row is compared with the input search key using each set of respective mask pointer pairs, each of the pointer pairs is selected to correspond to the smallest mask for which the input search key equals the maximum key in a row of a corresponding lookup table with the corresponding number of mask bits ignored. Applicants see no mention of a mask, as claimed in this section of Bass and would like the Examiner to specify where these features are disclosed by Bass. Furthermore, if no match of a leaf is found in Bass a not OK value is returned (se column 26, lines 1-5), in contrast to the claim 9, which selects a maximum key. Moreover while Bass mentions a largest prefix match type tree search in column 25, line 49, there is no mention as to the details of what Bass is referring to here. Accordingly, Applicants respectfully request that the Examiner specify where the longest prefix match details as specified in claim 9 exist in Bass rather than a brief mention of a similar acronym.

For at least the above stated reasons, claims 1, 5, and 8 are patentable over the cited combination of references. Similarly, claims 2-4, 6-7, and 9-11 are also patentable over the cited references.

In view of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. A notice of allowance is respectfully requested. In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at **(408) 774-6921**. If any fees are due in connection with the

filing of this paper, then the Commissioner is authorized to charge such fees to Deposit Account No. 50-0805 (Order No. ALTEP068). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, L.L.P.



Michael L. Gencarella, Esq.
Reg. No. 44,703

MARTINE PENILLA & GENCARELLA, L.L.P.
710 Lakeway Drive, Suite 200
Sunnyvale, California 94085
Telephone: (408) 749-6900
Customer Number 45640